

**P- Channel 60-V (D-S) MOSFET**

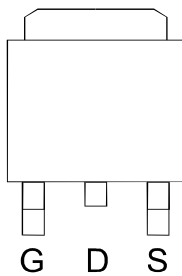
**GENERAL DESCRIPTION**

The ME20P06 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

**PIN CONFIGURATION**

(TO-252-3L)

Top View

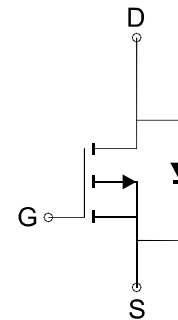


**FEATURES**

- $R_{DS(ON)} \leq 78m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 100m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



P-Channel MOSFET

**Ordering Information:** ME20P06 (Pb-free)

ME20P06-G (Green product-Halogen free )

**Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain	$I_D$	$T_c = 25^\circ C$	-17.7
		$T_c = 70^\circ C$	-14.1
Pulsed Drain Current	$I_{DM}$	-71	A
Maximum Power Dissipation	$P_D$	$T_c = 25^\circ C$	39.1
		$T_c = 70^\circ C$	25
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	3.2	$^\circ C/W$

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper



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### Electrical Characteristics (T<sub>c</sub> =25°C Unless Otherwise Specified)

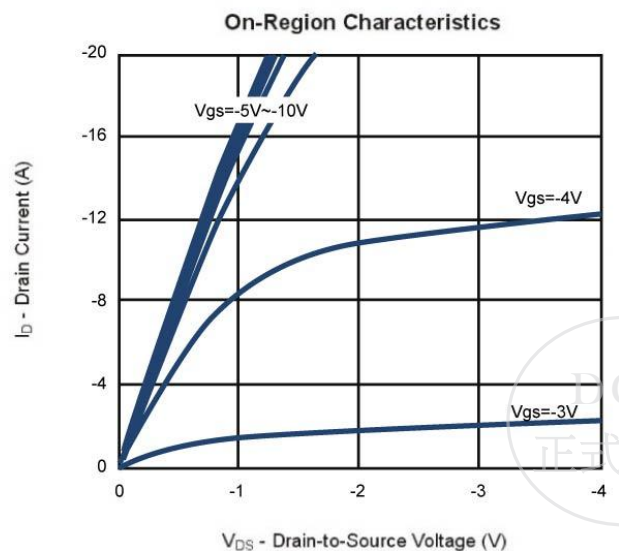
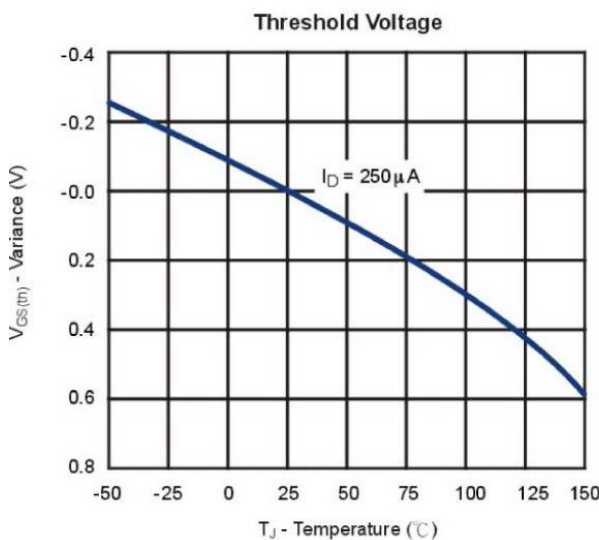
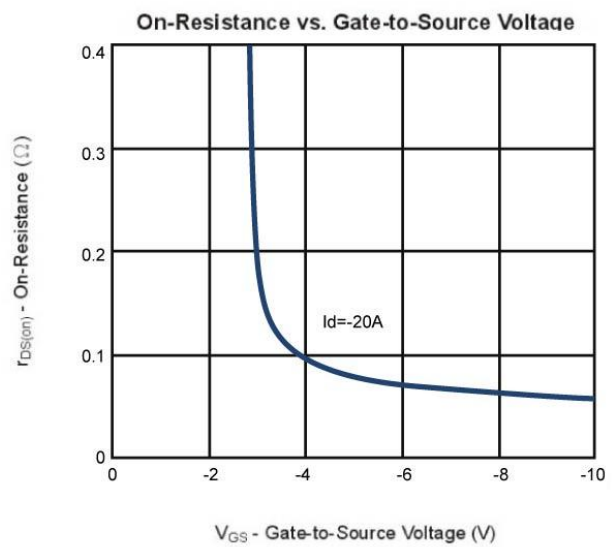
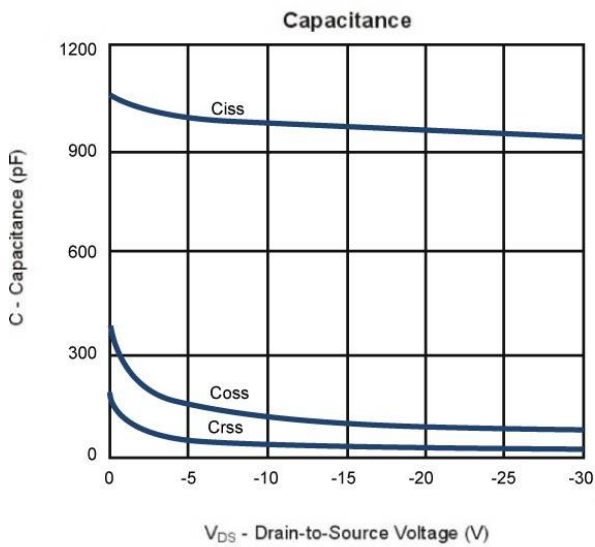
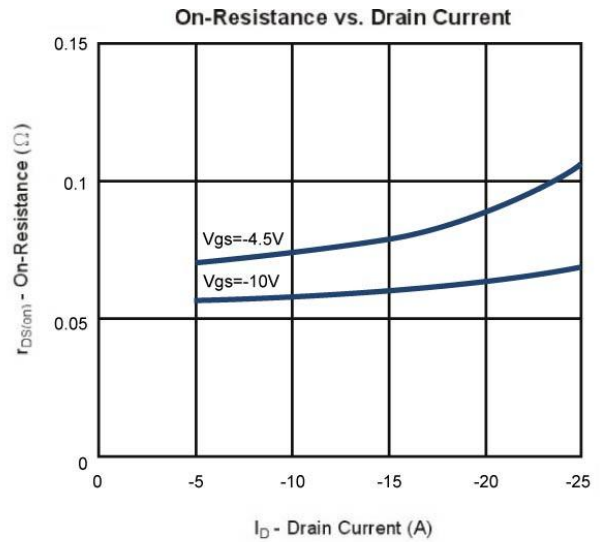
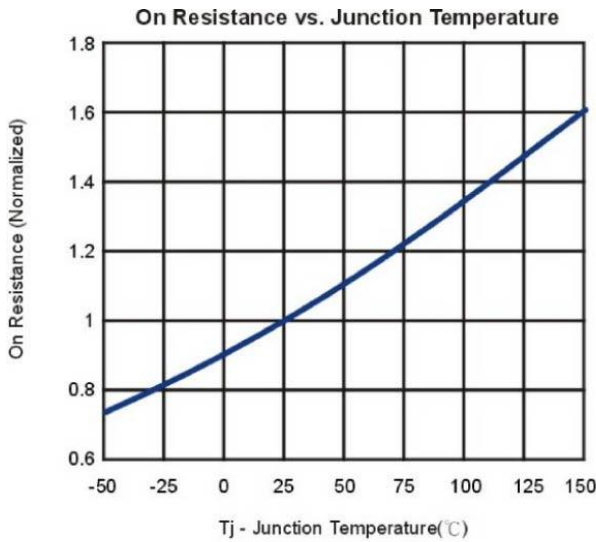
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250 μA	-60			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250 μA	-1		-3	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V			-1	μA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>a</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> = -20A		65	78	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> = -16A		80	100	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V		-1	-1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge(10V)	V <sub>DS</sub> =-30V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A		22		nC
Q <sub>g</sub>	Total Gate Charge(4.5V)	V <sub>DS</sub> =-30V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A		10		
Q <sub>gs</sub>	Gate-Source Charge			6.3		
Q <sub>gd</sub>	Gate-Drain Charge			5		
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, F=1MHz		958		pF
C <sub>oss</sub>	Output Capacitance			100		
C <sub>rss</sub>	Reverse Transfer Capacitance			33		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =-15V, R <sub>L</sub> =15Ω I <sub>D</sub> =-1A, V <sub>GEN</sub> =-10V, R <sub>G</sub> =3Ω		36		ns
t <sub>r</sub>	Turn-On Rise Time			16		
t <sub>d(off)</sub>	Turn-Off Delay Time			53		
t <sub>f</sub>	Turn-Off Fall Time			6		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

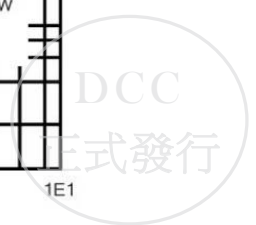
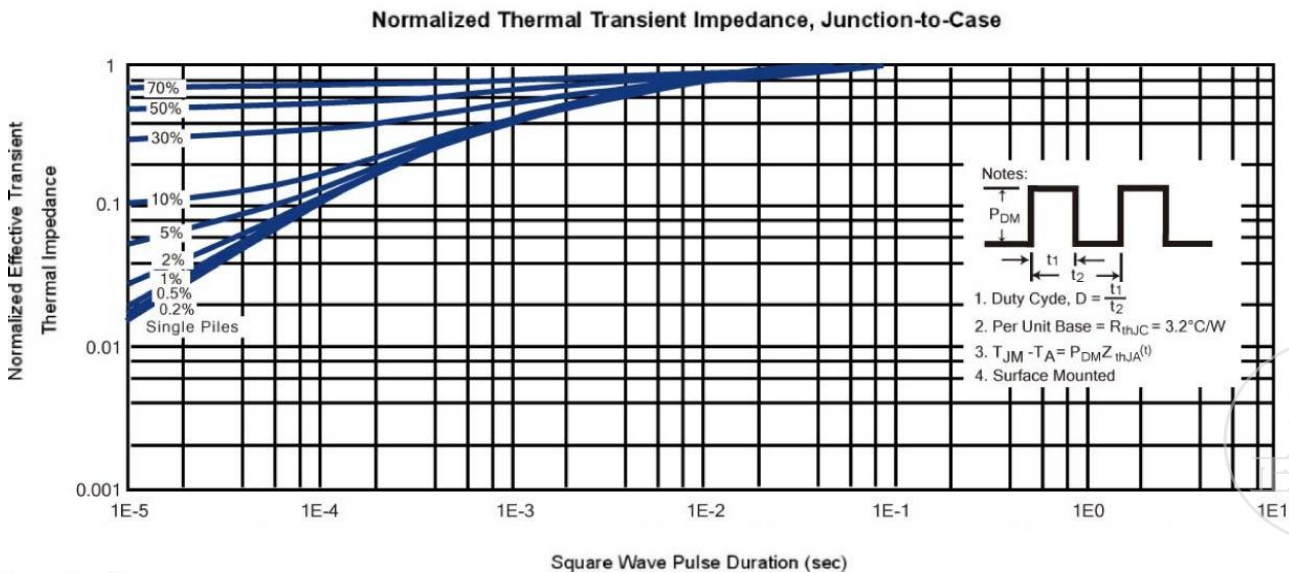
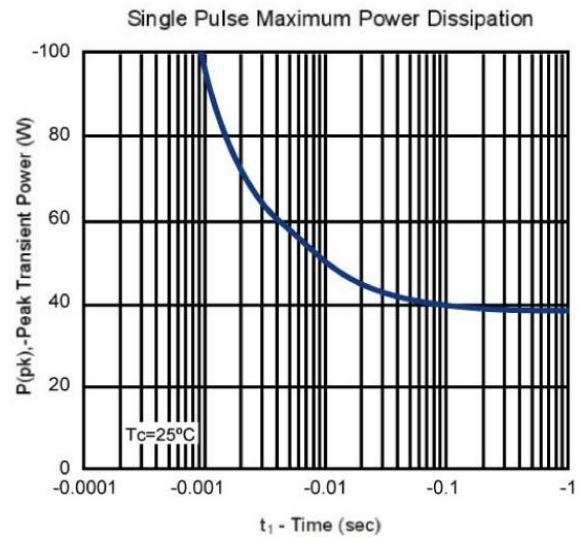
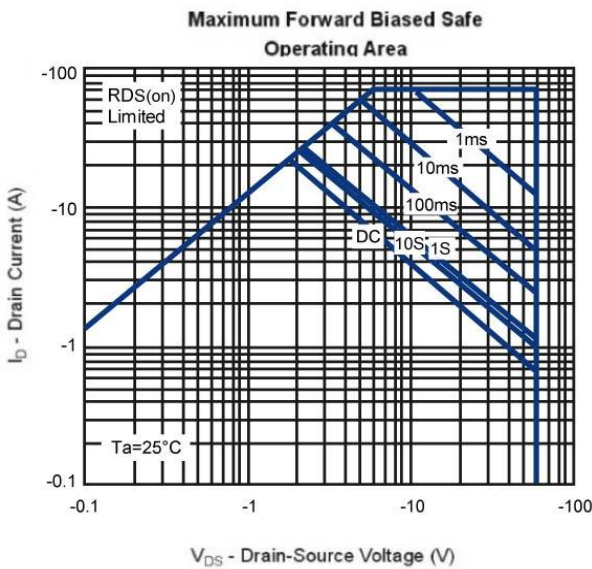
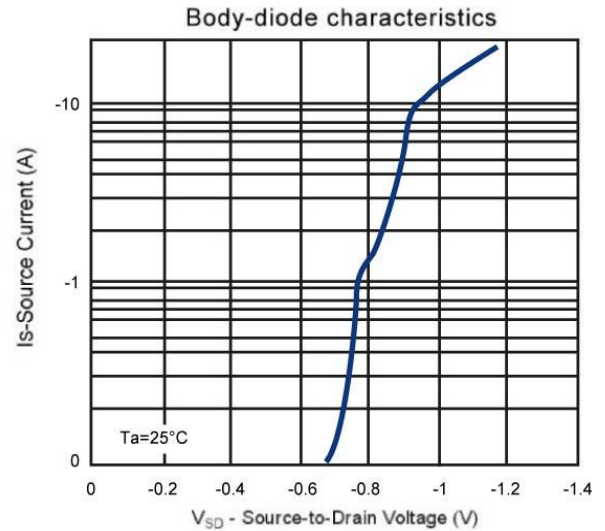
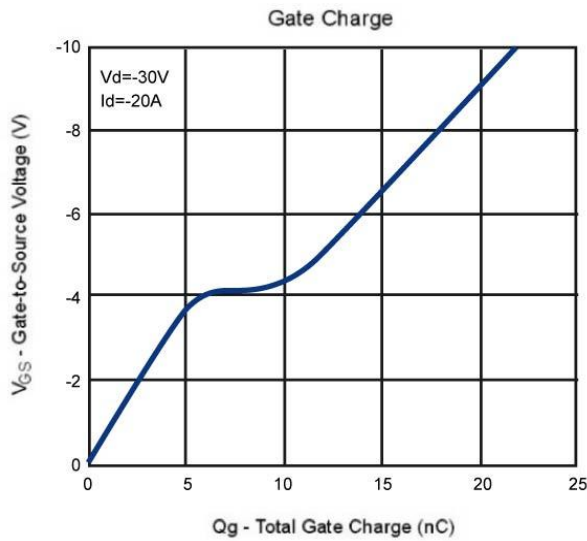
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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**P- Channel 60-V (D-S) MOSFET**  
**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

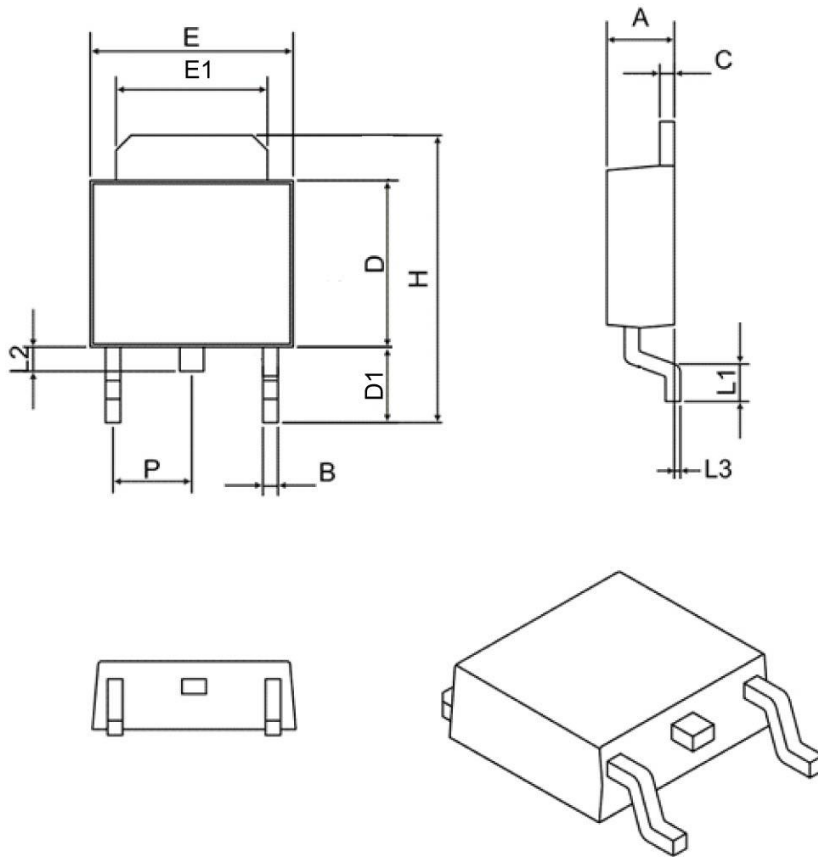


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**TO252-3L Package Outline**



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

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